**Lab 10**

**To Design and Implement Multiplexer & Demultiplexer**

**Tasks**

1. **Construct a logic circuit for 8 to 1 multiplexer with the help of truth table. Also write the Boolean expression for output(s). Simulate your circuit to verify the outputs.**

8 to 1 Mux

1. Block Diagram

**D0**

**D1**

**D2**

**Q**

**D3**

**8 to 1**

**MUX**

**D4**

**D5**

**D6**

**D7**

**S0**

**S1**

**S2**

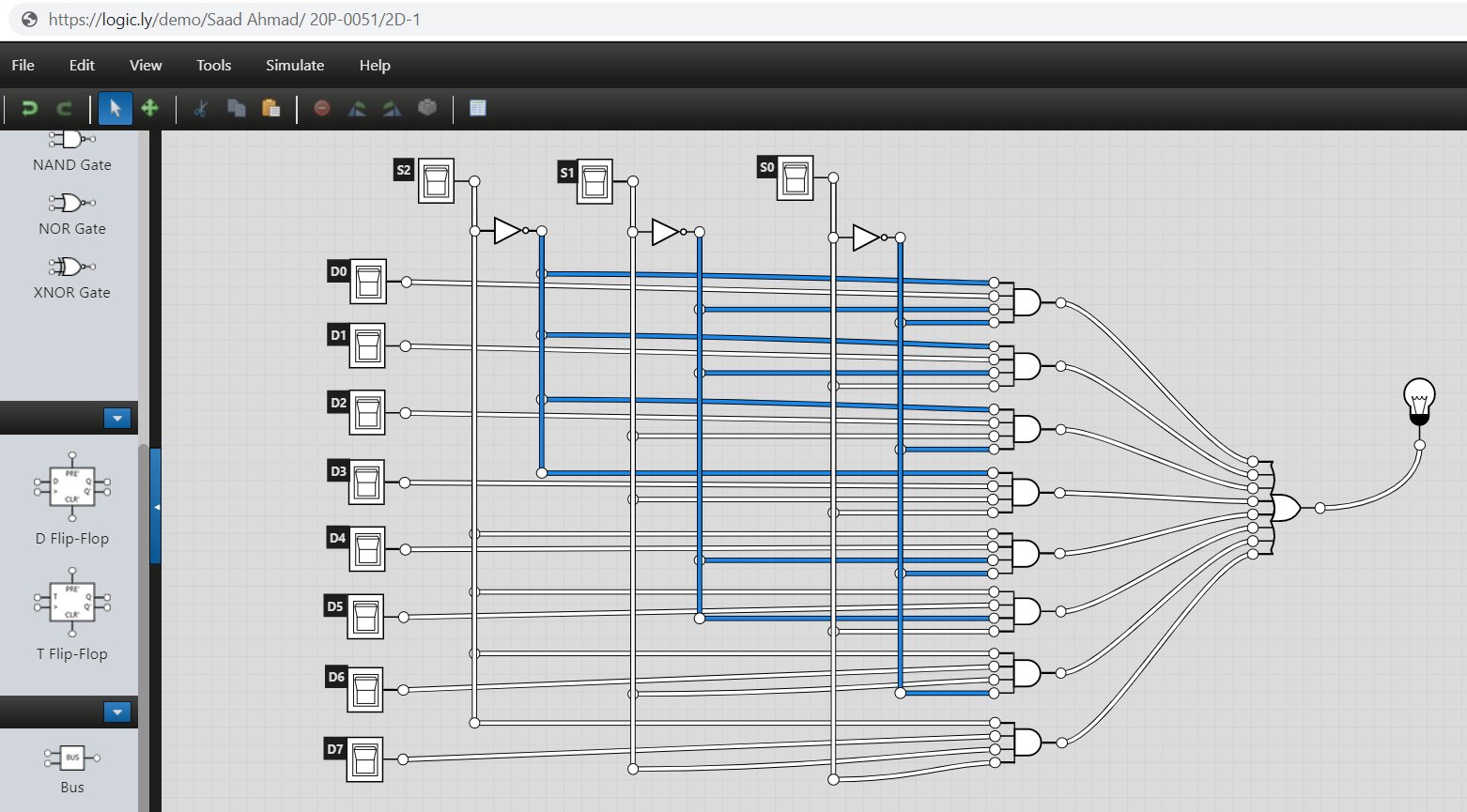
1. Truth Table

|  |  |  |  |
| --- | --- | --- | --- |
| **S2** | **S1** | **S1** | **Q** |
| **0** | **0** | **0** | **D0** |
| **0** | **0** | **1** | **D1** |
| **0** | **1** | **0** | **D2** |
| **0** | **1** | **1** | **D3** |
| **1** | **0** | **0** | **D4** |
| **1** | **0** | **1** | **D5** |
| **1** | **1** | **0** | **D6** |
| **1** | **1** | **1** | **D7** |

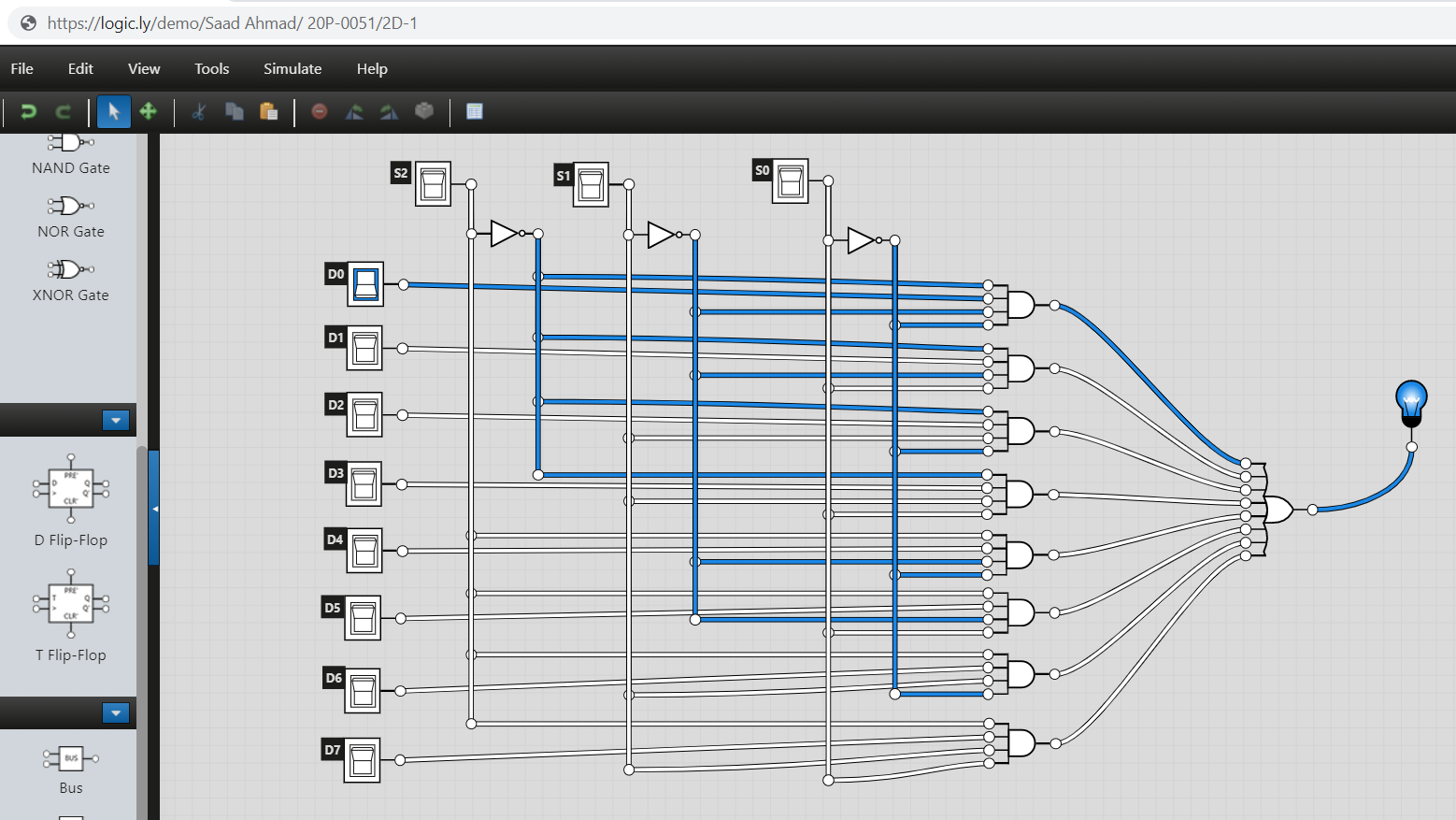
1. Boolean Expression

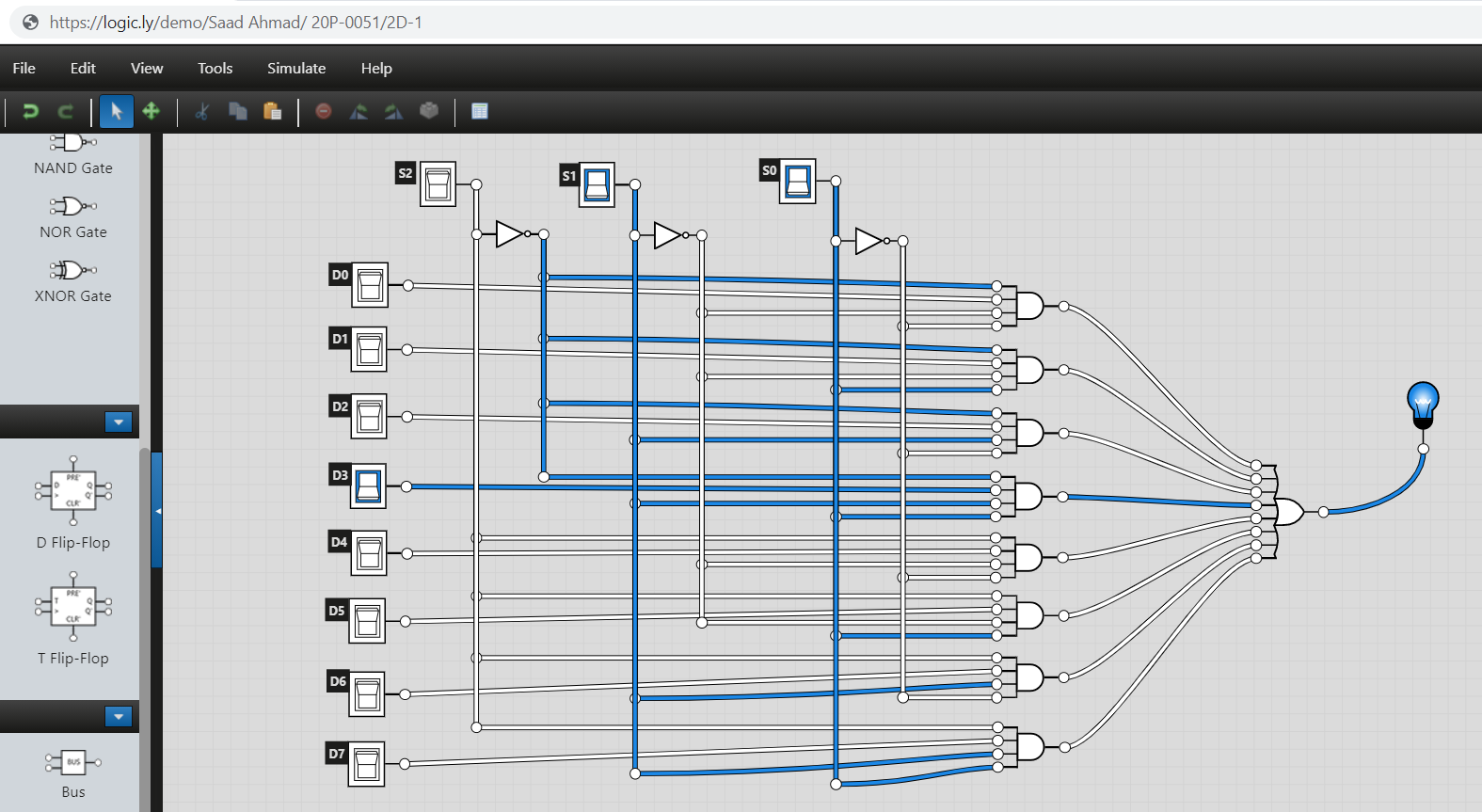
Q = S2’.S1’.S0’.D0 + S2’.S1’.S0.D1 + S2’.S1.S0’.D2 + S2’.S1.S0.D3 + S2.S1’.S0’.D4 + S2.S1’.S0.D5 + S2.S1.S0’.D6 + S2.S1.S0.D7

1. Logic Diagram (from logicaly or hand drawn)



1. Software Simulation





1. **Design a logic circuit for 1-to-4-line Demultiplexer. Also write the Boolean expression for output(s). Simulate your circuit to verify the outputs.**
2. Block Diagram

**D0**

**D1**

**1 to 4**

**DEMUX**

**D3**

**D2**

**Q**

**S1**

**S0**

1. Truth Table

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Q |
| 0 | 0 | D0 |
| 0 | 1 | D1 |
| 1 | 0 | D2 |
| 1 | 1 | D3 |

1. Boolean Expression

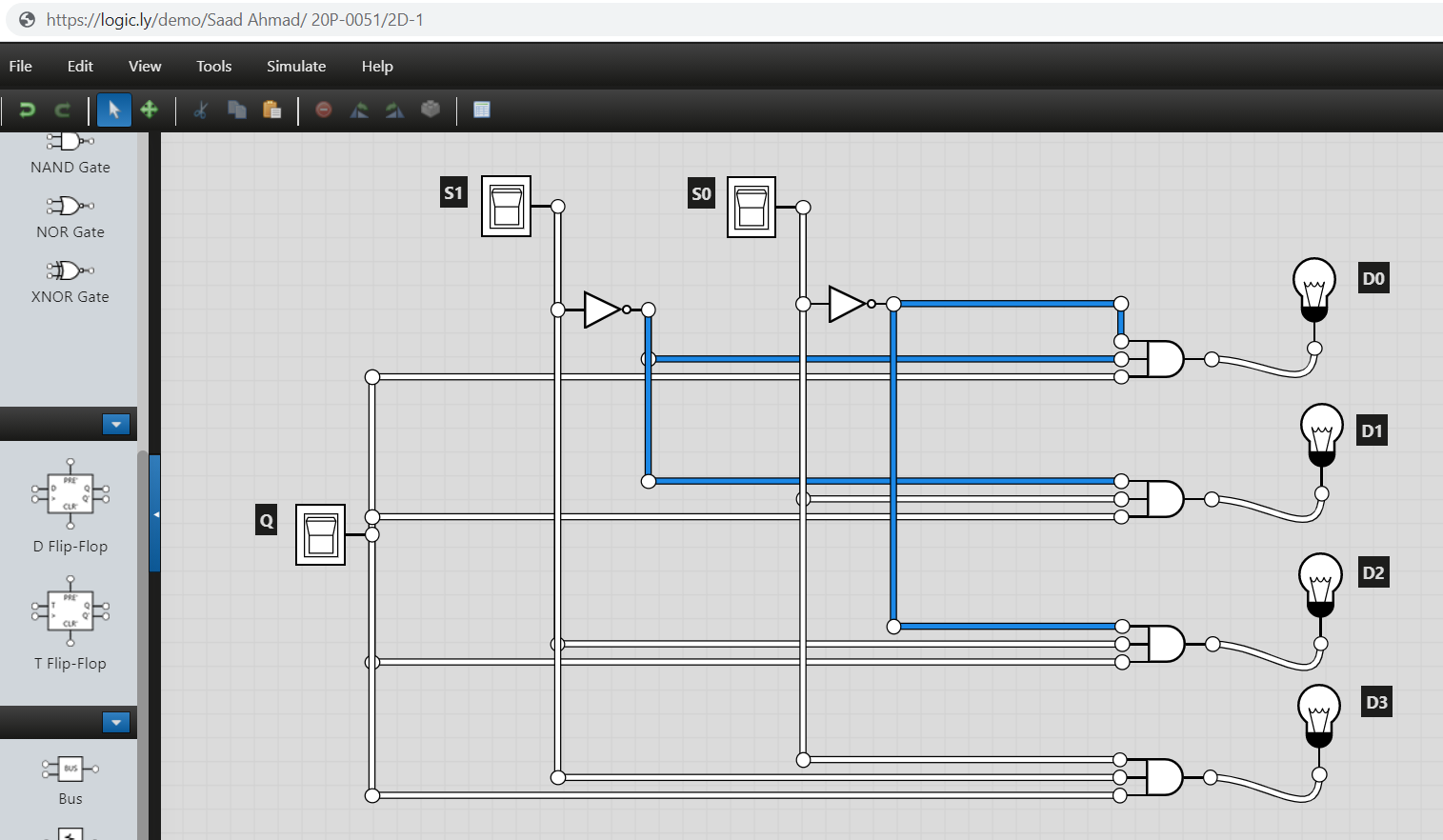
D0 = S1’. S0’. Q

D1 = S1’. S0. Q

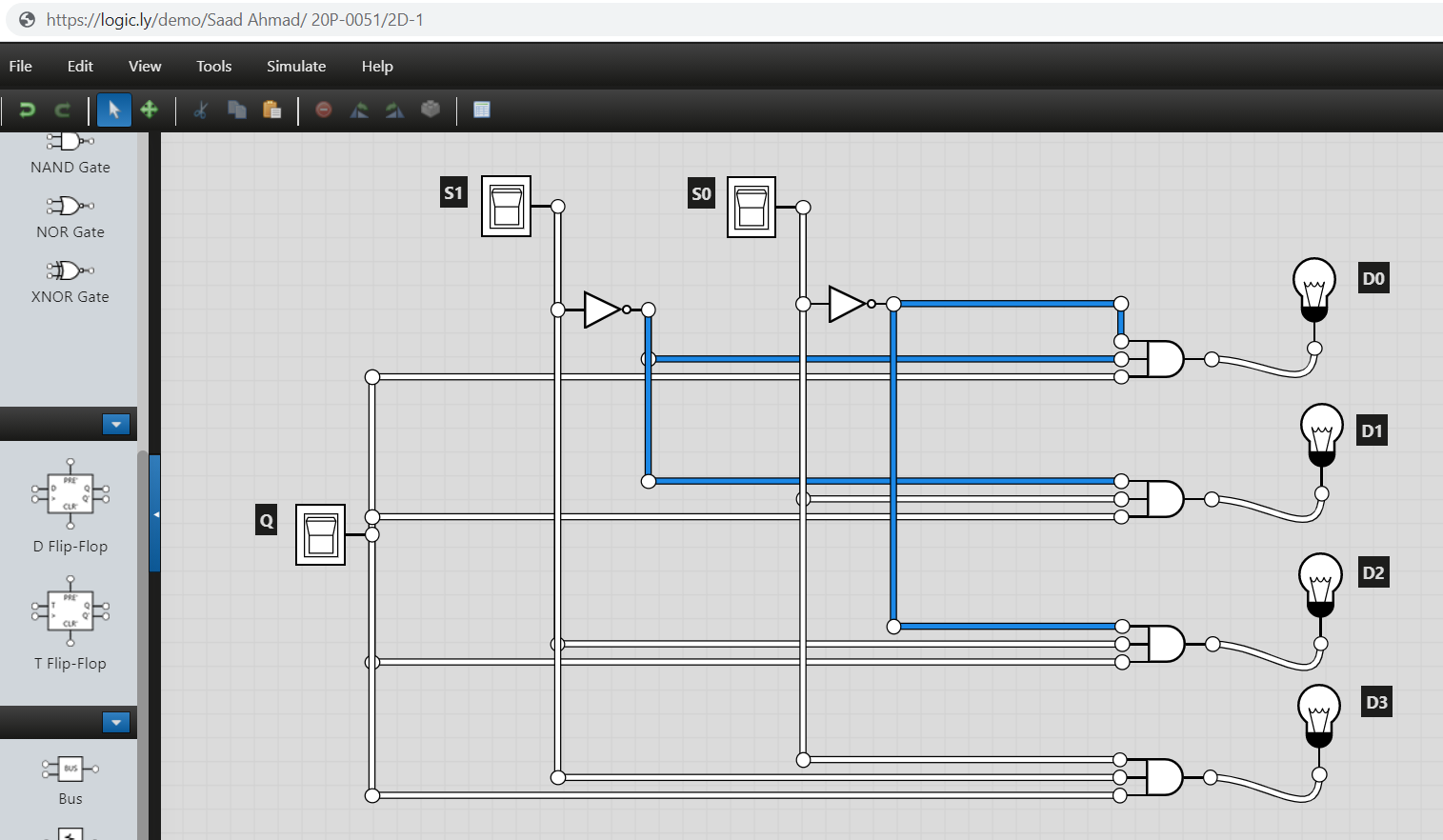
D2 = S1. S0’. Q

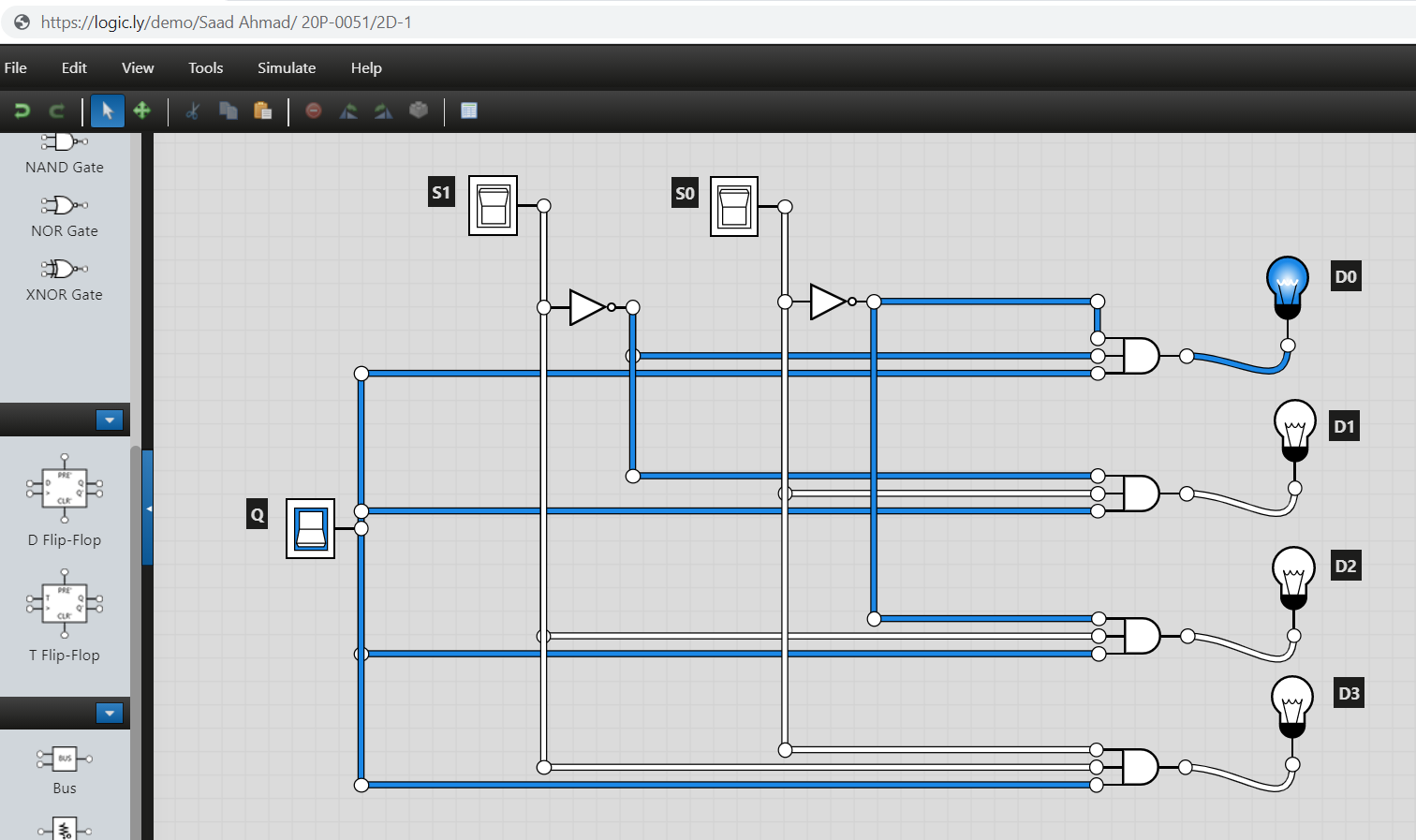
D3 = S1. S0. Q

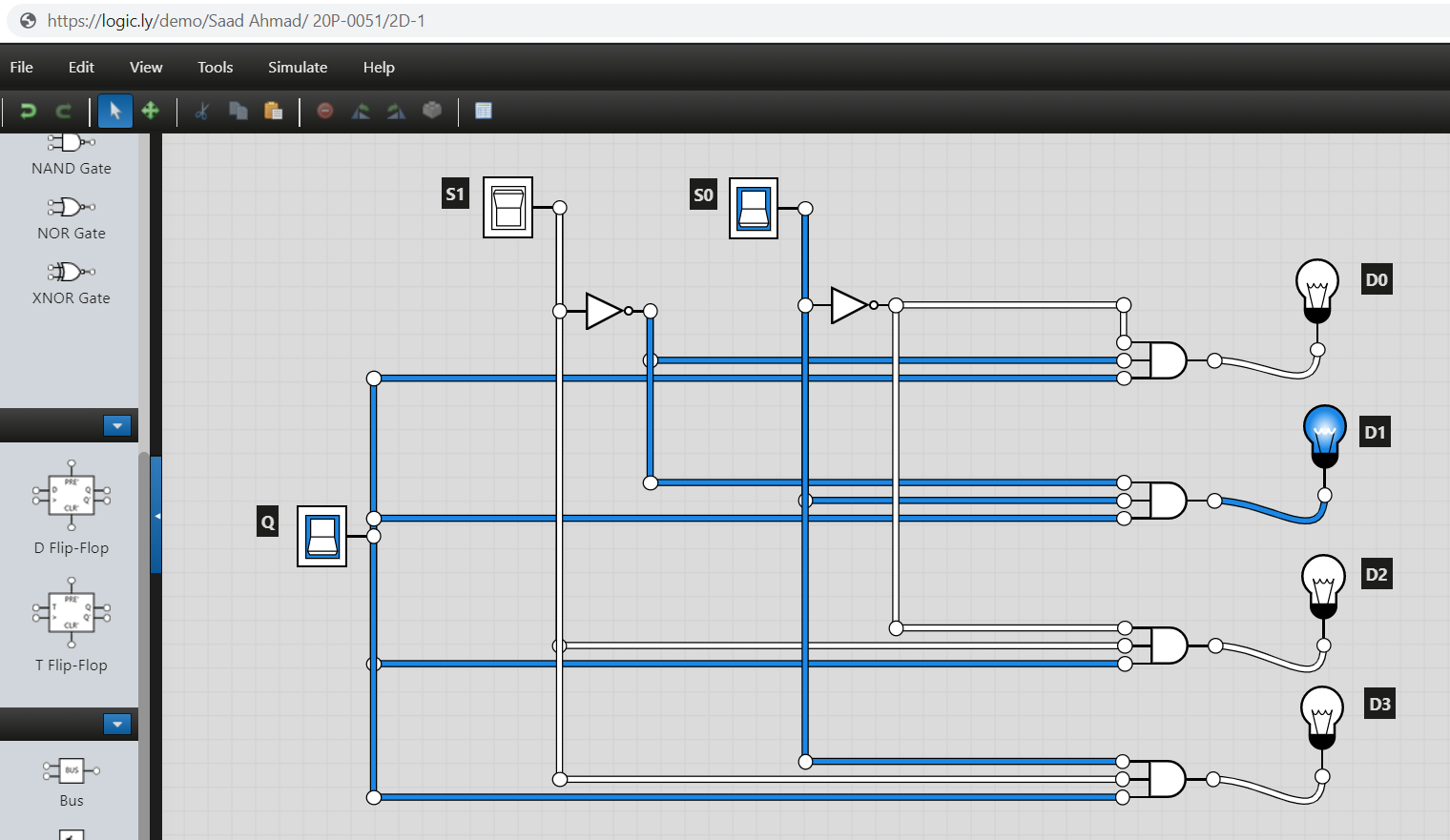
1. Logic Diagram



1. Software Simulation







1. **Design a circuit for 4 to 1 Multiplexer using 2 to 1 Multiplexer(s). You can take help from google or the link below. Just ignore the coding language discussed in the link.**

*https://bravelearn.com/design-of-4x2-multiplexer-using-2x1-mux-in-verilog/*

1. Block Diagram

**S0**

**S1**

**2 x 1 MUX**

**Q**

**2 x 1 MUX**

**S3**

**S4**

**2 x 1 MUX**

**S0**

**S1**

1. Truth Table

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Q |
| 0 | 0 | D0 |
| 0 | 1 | D1 |
| 1 | 0 | D2 |
| 1 | 1 | D3 |

1. Logic Circuit (on the basis of 2 to 1 Muxes used/follow the block diagram to draw this circuit)

*You need to connect three* ***2 x1 Multiplexers*** *in order to make one* ***4x1 Multiplexer****.*

